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PTO/SB/21 (09-04)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/630,249
Filing Date	July 30, 2003
First Named Inventor	Mo, Brian S.
Art Unit	2811
Examiner Name	HA, Nathan W.
Attorney Docket Number	018865-001740US
Total Number of Pages in This Submission	35

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
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- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [ ] Appeal Communication to Board of Appeals and Interferences
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- [ ] Proprietary Information
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- [x] Other Enclosure(s) (please identify below):

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Firm Name	Townsend and Townsend and Crew LLP		
Signature	[signature]		
Printed name	Babak S. Sani		
Date	Nov. 3, 2005	Reg. No.	37,495

CERTIFICATE OF TRANSMISSION/MAILING

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PTO/SB/17 (12-04)

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500

Complete if Known	
Application Number	10/630,249
Filing Date	July 30, 2003
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Art Unit	2811
Attorney Docket No.	018865-001740US

METHOD OF PAYMENT (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims ______ -20 or HP = **Extra Claims** ______ x **Fee ($)** ______ = **Fee Paid ($)** ______

HP = highest number of total claims paid for, if greater than 20

Multiple Dependent Claims **Fee ($)** ______ **Fee Paid ($)** ______

Indep. Claims ______ -3 or HP = **Extra Claims** ______ x **Fee ($)** ______ = **Fee Paid ($)** ______

HP = highest number of independent claims paid for, if greater than 3

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets ______ - 100 = **Extra Sheets** ______ / 50 = **Number of each additional 50 or fraction thereof** ______ (round **up** to a whole number) x **Fee ($)** ______ = **Fee Paid ($)** ______

4. OTHER FEE(S) **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount) ______

Other: Filing a brief in support of an appeal 500

SUBMITTED BY

Signature	Babak S. Sani	Registration No. (Attorney/Agent) 37,495	Telephone 415-576-0200
Name (Print/Type)	Babak S. Sani		Date Nov. 3, 2005

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By: [signature]

PATENT
Attorney Docket No.: 018865-001740US
Client Ref. No. 17732-7226.001.001

OIPE IAP15
NOV 07 2005
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:

MO et al.

Application No.: 10/630,249

Filed: July 30, 2003

For: FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE

Customer No.: 20350

Confirmation No. 9390

Examiner: HA, Nathan W.

Technology Center/Art Unit: 2811

APPEAL BRIEF

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Sir:

Appellants offer this Brief further to the Notice of Appeal mailed on September 1, 2005.

11/07/2005 SSITHIB1 00000124 201430 10630249

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I. REAL PARTY IN INTEREST

Fairchild Semiconductor Corporation is the real party in interest as the assignee of the present patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

III. STATUS OF CLAIMS

Claims 46-120 are currently pending in the application. All pending claims stand finally rejected pursuant to a final Office Action mailed May 3, 2005. The rejections of the claims are believed improper and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments have been entered subsequent to the final Office Action mailed May 3, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In the following summary, Appellants have provided exemplary references to sections of the specification and drawings supporting the subject matter defined in the claims as required by 37 C.F.R. § 41.37. The specifications and drawings also include additional support for other exemplary embodiments encompassed by the claimed subject matter. Thus, these references are intended to be illustrative in nature only.

Power devices such as MOSFETs (metal oxide semiconductor field effect transistors) are well known in the semiconductor industry. The DMOS (double diffused metal oxide semiconductor) field effect transistor is a power device that typically includes a substrate, an epitaxial layer, a doped well, a doped source junction formed inside the well and a gate electrode. The gate electrode can be formed either on the top surface in a planar fashion or inside a trench. When voltage is applied to the gate electrode current flows vertically from the source region down to the substrate which acts as the drain terminal.

One performance criteria for the power MOSFET is the transistor breakdown voltage. In a trench-gated MOSFET, to improve breakdown voltage, it is desirable to move the

location of peak electric field away from trench corners. The provision of a deep, heavily doped body region that is deeper than the well or the trench and located between trenches has been a common method of moving the peak electric field away from trench corner. Forming the deeper heavy body, however, increases the spacing between trenches which results in lower cell density and increased transistor on resistance.

In one embodiment of the present invention, a trench gated transistor includes a heavy body formed inside the well. The heavy body is shallower than the bottom of the trench and forms an abrupt junction at the interface with the well. In another embodiment of the present invention, a trench gated transistor includes a heavy body formed inside the well. The heavy body is shallower than the bottom of the trench and has a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate. When voltage is applied to the transistor, the structure of the heavy body causes the peak electric field to occur in the area of the bottom of the heavy body and away from the trench corners. The resulting device exhibits improved breakdown voltage without compromising cell density or transistor on resistance.

Independent claim 46

The embodiment of independent claim 46 discloses a field effect transistor comprising a semiconductor substrate having dopants of a first conductivity type and a trench extending a predetermined depth into the substrate. *Application*, page 6, lines 4-6, Figs.1A and 1B. The field effect transistor also comprises a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the substrate to form a well junction at a first depth. *Id.*, page 6, lines 11-12, Figs. 1A and 1B. The field effect transistor also comprises a doped source region having dopants of the first conductivity type and extending into the substrate to form a source junction at a second depth. *Id.*, page 6, lines 9-10, Figs. 1A and 1B. The field effect transistor also comprises a doped heavy body region having dopants of the second conductivity type and extending into the doped well to form a heavy body junction at a depth that is deeper than the source junction and shallower than the trench, wherein the heavy body forms an abrupt junction in the doped well. *Id.*, page 6, lines 9-10 and 29-30, Figs. 1A and 1B.

Independent claim 67

The embodiment of independent claim 67 discloses a field effect transistor comprising a semiconductor substrate having dopants of a first conductivity type and a trench extending a predetermined depth into the substrate. *Id.*, page 6, lines 4-6, Figs.1A and 1B. The field effect transistor also comprises a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into the substrate, the space between adjacent trenches defining a contact area. *Id.*, page 5, line 32 to page 6, line 1, Fig. 1. The field effect transistor also comprises a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the substrate to form a well junction with the substrate. *Id.*, page 6, lines 11-12, Figs. 1A and 1B. The field effect transistor also comprises a doped source region having dopants of the first conductivity type forming a source junction inside the doped well. *Id.*, page 6, lines 9-10, Figs. 1A and 1B. The field effect transistor also comprises a heavy body having dopants of the second conductivity type and extending into the doped well to a second depth that is deeper than the source junction. *Id.*, page 6, lines 9-10 and 29-30, Figs. 1A and 1B. The field effect transistor also comprises heavy body contact regions defined at the surface of the substrate along the length of the contact area. *Id.*, page 5, line 33 to page 6, line 1, Fig. 1. The heavy body forms an abrupt junction within the doped well. *Id.*, page 6, lines 9-10 and 29-30, Figs. 1A and 1B.

Independent claim 97

The embodiment of independent claim 97 discloses a field effect transistor comprising a semiconductor substrate having dopants of a first conductivity type and a trench extending a predetermined depth into the substrate. *Id.*, page 6, lines 4-6, Figs.1A and 1B. The field effect transistor also comprises a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the substrate to form a well junction at a first depth. *Id.*, page 6, lines 11-12, Figs. 1A and 1B. The field effect transistor also comprises a doped source region having dopants of the first conductivity type and extending into the substrate to form a source junction at a second depth. *Id.*, page 6, lines 9-10, Figs. 1A and 1B. The field effect transistor also comprises a doped heavy body region having dopants of the second conductivity type and extending into the doped well to form a heavy body junction at a

depth that is deeper than the source junction and shallower than the trench, the doped heavy body region having a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate. *Id.*, page 9, lines 23-28, Fig. 5.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 46-52, 54-58, 60-65, 67-73, 84, 86-87, 89, 92-95, 97-103, 105-109, 111-113, and 118 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,689,128 to Hshieh et al. (hereinafter "Hshieh").

B. Claims 53, 59, 74-73, 85, 88, 90-91, 96, 104, 110, and 119-120 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hshieh in view of U.S. Patent No. 6,204,533 to Williams et al. (hereinafter "Williams").

VII. ARGUMENT

A. Hshieh fails to anticipate claims 46-52, 54-58, 60-65, 67-73, 84, 86-87, 89, 92-95, 97-103, 105-109, 111-113, and 118 under 35 U.S.C. § 102(e)

Claims 46-52, 54-58, 60-65, 67-73, 84, 86-87, 89, 92-95, 97-103, 105-109, 111-113, and 118 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hshieh. "Under 35 U.S.C. 102, anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference…." *Akzo v. N.V. v. U.S. Int'l Trade Comm'n,* 808 F.2d 1471, 1 USPQ2d 1241 (Fed. Cir. 1986) *cert. denied*, 482 U.S. 909 (1987). Appellants respectfully submit that Hshieh does not disclose each and every element of the rejected claims, and that the claims can be distinguished from Hshieh in a number of respects.

1. <u>Claims 46-96: Hshieh fails to disclose an "abrupt junction"</u>

All claims 46-96 recite a heavy body region that forms an "abrupt junction" in a doped well. With respect to this feature, the Examiner states that the "heavy body region inherently forms an abrupt junction in the doped well." Appellants respectfully traverse.

(a) Examiner has not met the burden of proof for inherency

It is well established that for a prior art reference to inherently disclose a missing descriptive matter, the Examiner must provide objective evidence or cogent technical reasoning to show that the missing descriptive matter is necessarily present in the device described in the reference. MPEP [2112 IV]. "In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic <u>necessarily</u> flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

The only technical reasoning provided by the Examiner in support of the inherency allegation is that "the cited art discloses a structure of the device that is identical with the instant application's device." Appellants submit that not only are none of the devices disclosed in Hshieh identical to the claimed device, but that the very same structural differences establish that Hshieh did not even contemplate the use of an abrupt junction.

For example, all three embodiments described by Hshieh (and shown in Figs. 1, 2, and 3) have structural features that are not only different but are the critical aspects of the Hshieh devices that provide the purported improvements in breakdown voltage. Specifically, the structural differences include: with respect to Hshieh's Fig. 1 embodiment, a "P+ deep body region" 36 that is deeper than the well 14 and the trench 24 [Col. 3, lines 1 *et seq.*]; with respect to Hshieh's Fig. 2 embodiment, a "P+ deep body region"36 that is deeper than the well 14 and extends into "a second (upper) epitaxial layer (drift region) 34" [Col. 2, lines 63 *et seq.*]; and with respect to Hshieh's Fig. 3 embodiment, the same double epitaxial structure without the deep P+ body region. [Col. 4, lines 14-23].

None of the devices of the present invention has a "deep" heavy body (whether deeper than the well or deeper than the trench) nor a double-epitaxial layer, and therefore all differ from the devices disclosed in Hshieh in significant respects. That is, the present invention neither employs a P region *deeper than the trench* (Fig. 1 in Hshieh), nor a *double epitaxial layer* underlying the P region (Figs. 2 and 3 in Hshieh). Instead, the present invention employs in one embodiment a heavy body region 34 that is shallower than the trench 26 and forms an abrupt junction inside the well 36.

Thus, contrary to the Examiner's assertion, the structure of the device of the present invention is clearly not "identical" to any of the structures shown in Hshieh. Accordingly, because no objective evidence or cogent technical reasoning has been offered to show that the missing descriptive matter is necessarily present in the device described in Hshieh, the Examiner has failed to meet the burden of proof for establishing inherency.

(b) Abrupt junction is not "necessarily" present in Hshieh

Even if it is determined that the Examiner has provided an objective basis in fact or technical reasoning to reasonably support a *prima facie* case of inherency, such *prima facie* case of inherency can be rebutted by evidence showing that the prior art products do not <u>necessarily</u> possess the characteristics of the claimed product." [MPEP 2112.01, Chapter I]. Appellants respectfully submit that the abrupt junction is not necessarily present in Hshieh for at least the following reasons.

First, it should be noted that absent any explicit information about the nature of a diffused junction, one skilled in the art of semiconductor processing would not assume the nature of the junction to be abrupt. To one of skill in this art, an "abrupt" junction defines a particular type of junction with specific features that is distinct from a "linearly graded" junction. This distinction in terms of structure and properties between the abrupt junction and the linearly graded junction is thoroughly analyzed, for example, in S.M. Sze's seminal book titled "Physics of Semiconductor Devices," under section 2.3.1 titled "Abrupt Junction." Sze explains that whether a junction is abrupt or linearly graded depends on a number of different but inter-dependent variables, including background doping concentration, target breakdown voltage, etc.

Second, not only is the "abrupt" junction a distinct type of junction that cannot be simply assumed to exist in every junction, but the more common type of junction is the "linearly graded" junction because it typically results from commonly employed diffusion processes. The abrupt junction, on the other hand, typically requires additional processing steps (*e.g.*, double implant) or other types of specific processing variations. Thus, because of these significant differences in structure, properties and processing requirements, a junction is more commonly assumed to be linearly graded unless expressly defined as "abrupt." A linearly graded junction would be the appropriate assumption made by one of ordinary skill in the art reading Hshieh.

Third, it is apparent that the abrupt junction between the heavy body and the well was not even contemplated by Hshieh for the purpose of improving the breakdown voltage. Hshieh attempts to address the same problem the present invention does, but none of its three disclosed embodiments even remotely suggests that an abrupt junction may help in addressing the problem of breakdown voltage. Instead Hshieh offers distinctly different structural features to address the same problem, demonstrating that Hshieh did not even contemplate the use of an abrupt junction.

For example, the first embodiment in Hshieh (Fig. 1) is directed at the fabrication of P+ deep body regions that extend deeper than the bottom of the trench. The characteristic that improves breakdown voltage for the embodiment of Fig. 1 is stated to be the placement of the P+ deep body region deeper than the trench. Hshieh states that for such a structure, "in order to avoid destructive breakdown occurring at the bottom of the trench... such transistors are *fabricated so that a P+ deep body region extends deeper than does the bottom of the trench.*" [Col. 1, lines 28-30]. Thus, the embodiment in Fig. 1 of Hshieh clearly neither contemplates nor suggests an abrupt junction for the P+ deep body junction.

Regarding the second embodiment (Fig. 2), Hshieh states: "a double epitaxial layer is provided underlying the body region, with the P+ region not extending below the depth of the trench. *Instead, the double epitaxial layer* provides the desired current path away from the bottom of the trenches." [Col. 2, lines 2-9, emphasis added]. Again, according to Hshieh a different structure (double epitaxial layer) is needed to improve breakdown voltage Accordingly, the embodiment shown in Fig. 2 of Hshieh neither contemplates nor suggest that an abrupt nature for the P+ deep body junction may serve to improve the problem of breakdown voltage.

The third embodiment in Hshieh (Fig. 3) is similar to the second, but without a P+ deep body and with only the double epitaxial layer. However, Hshieh discloses that the structure of Fig. 2 is likely to perform better than that of Fig. 3 because "the Fig. 3 transistor may have some residual problem of oxide rupture, i.e. destructive breakdown at the bottom of the trenches, due to the higher electric field between a P+ deep body region and the drain region 10." But had Hshieh even contemplated an *abrupt* junction between the heavy body and the well at a position shallower than the trench, there would have been no such concern for breakdown at the bottom

of the trenches for the structure of Fig. 3. The present invention, on the other hand, specifically utilizes in one embodiment the abruptness of the heavy body junction to improve breakdown voltage.

Accordingly, Hshieh clearly fails to inherently disclose an abrupt junction because not only does the use of an abrupt junction not necessarily flow from Hshieh's teachings, but Hshieh's teachings to use other, structurally distinct features to address the same problem that an abrupt junction helps address make clear that Hshieh did not even contemplate the use of an abrupt junction as claimed. All claims 46-96 are therefore distinguished from Hshieh for at least this reason.

2. <u>Claims 46-120: Hshieh fails to disclose a "heavy body" that is formed within the well and is deeper than the source</u>

All of the pending claims recite a "heavy body" that forms a junction inside the well and that is deeper than the source junction. In rejecting the claims under the first ground, in the final Office Action of May 3, 2005, the Examiner points to Fig. 3 of Hshieh and refers to "region 36 or 18" as teaching the claimed "heavy body." Appellants respectfully traverse.

(a) Region 36 in Fig. 2 of Hshieh

There is no region 36 in Fig. 3 of Hshieh. Appellants assume the Examiner refers to region 36 of Fig. 2 of Hshieh. Region 36 in Fig. 2 is described in Hshieh as a "P+ deep body region." [Col. 4, lines 1-7]. As clearly depicted in Fig. 2 of Hshieh, while region 36 is shallower than the trench (22/24), it is deeper than and extends below the well region 14. Hshieh's P+ deep body region 36, therefore, extends below the P-well region 14 and forms a junction with the underlying epitaxial layer 34.

In contrast to Hshieh's P+ deep body 36, every pending claim in the present application defines a "heavy body" region that is formed inside the well and that does not extend deeper than the well. Independent claim 46 forms the heavy body junction "<u>in</u> the doped well," independent claim 67 forms the heavy body junction "<u>within</u> the doped well," and independent claim 97 forms the heavy body junction "<u>with</u> the doped well." The claimed "heavy body" therefore does not form a junction with the underlying epitaxial layer as taught by Hshieh's P+

deep body region 36 in Fig. 2 since it is surrounded by or formed within the well region. This has appreciable impact on performance because deeper diffusion of the P+ junction requires increased spacing between trenches resulting in reduced cell density and increased transistor on resistance.

Accordingly, Appellants respectfully submit that contrary to the Examiner's assertion, Hshieh's P+ deep body region 36 does not disclosed the claimed "heavy body" that is formed within the well region.

(b) Region 18 in Fig. 3 of Hshieh

Region 18 appears in all of Hshieh's figures including Fig. 3 and is defined by Hshieh as a "P+ doped body contact region." [Col. 3, lines 37-39]. All pending claims in the instant application define the heavy body as being "deeper than the source junction." There is no statement in Hshieh that defines the contact region 18 as being "deeper than the source junction." To the contrary, dimensions provided by Hshieh suggest the opposite. Hshieh teaches: "Formed in the upper portion of the epitaxial layer 12 are N+ doped source regions 20, having a typical depth of 0.5 μm." [Col. 3, lines 31-33]. Hshieh also requires the contact region 18 to be formed "*immediately over* each P+ deep body region." [col. 3, line37-39, emphasis added]. Furthermore, Hshieh defines the depth of the P+ deep body region 36 in the embodiment shown in Fig. 2 as extending "approximately 0.5 μm from the principal surface of the semiconductor body. " [Col. 4, lines 2-4]. Accordingly, looking at Hshieh's figures and considering Hshieh's statement that "the cross-sections shown here are not drawn to scale but are intended to be illustrative," one must conclude that contact region 18 must be shallower than the source region 20, since it is by definition shallower than the P+ "deep" body region 36. [Col. 2, lines 55-56]. Thus, contrary to the Examiner's assertion, Hshieh's contact region 18 does not disclose the claimed heavy body since it is not deeper than the source region.

Accordingly, Appellants respectfully submit that Hshieh does not teach a "heavy body" region that is formed inside the well and is deeper than the source regions. All rejected claims 46-120 are therefore further distinguished from Hshieh for this additional reason.

3. Claims 65, 95 and 116: Hshieh fails to disclose the claimed "distance between a bottom of the doped heavy body to the doped well junction"

Claims 65, 95 and 116 specify that "a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5 μm to 1.5 μm." In rejecting these claims, the Examiner asserts that Hshieh's "Fig. 3 depicts this range since region 14 is 2.5 microns and heavily doped region 18 extends at least half way of the region 34." This rejection is flawed for a number of reasons.

First, region 14 in Fig. 3 of Hshieh is not and cannot be 2.5 microns. It is in connection with the embodiment shown in Fig. 1 (not Fig. 3) of Hshieh where it is explained: "Included as a part of the body region 14 is a P+ deep body region 16 which has a total depth from the principal surface of the semiconductor body of about 2.5 μm." [Hshieh, col. 3, lines 16-19]. Therefore it is the deep P+ region 16 in Fig. 1 of Hshieh that is 2.5 microns deep and not the P doped body region 14 in Fig. 3. If P doped body region 14 were 2.5 microns there would be no transistor formed since the trenches are only 1-2 microns deep. [Hshieh, col. 3, lines 25-26]. That is, in order for the transistor gate (formed inside the trench) to overlap both the source region (18) and drain region (34/12/10) between which a channel is formed, P doped body region 14 must be shallower than the trench, and therefore cannot be as deep as the deep P+ region 16 (or 2.5 μm).

Second, as Appellants have already pointed out, Hshieh itself acknowledges that "the cross-sections shown here are not drawn to scale." [Col. 2, line 55]. Compare in the Hshieh figures, for example, source region 20 which is described at column 3, line 32 as having a "typical depth of 0.5 μm", to P+ deep body region 36 in Fig. 2 which is also described as "only [extending] approximately 0.5 μm from the principal surface of the semiconductor body." Yet in Fig. 2 of Hshieh the P+ deep body region 36 is depicted as being noticeably deeper than source regions 20. It is therefore improper to derive specific dimensions from the figures as the Examiner does when stating "Fig. 3 depicts this range since region 14 is 2.5 microns and heavily doped region 18 extends at least half way of the region 34." In fact, nowhere in Hshieh are there any specific dimensions provided either for the depth of the P+ region 18 or for the depth of the P doped region 14.

Accordingly, Hshieh fails to disclose the claimed distance between the bottom of the heavy body and the well junction. Claims 65, 95 and 116 are therefore further distinguished from Hshieh for this additional reason.

4. <u>Claims 67-96: Hshieh fails to disclose the "plurality of gate-forming trenches arranged substantially parallel to each other"</u>

Hshieh fails to anticipate claim 67-96 because Hshieh does not teach "a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate." This aspect of the invention is depicted in Figure 1 of the instant application, where trenches 14 extend in a striped, parallel fashion, or in what is commonly referred to as an "open cell" structure. There is no reference to this type of claimed structure anywhere in Hshieh. The closest Hshieh comes to defining an array is at Col. 2, lines 45 *et seq.*, where it states, "[it] is to be understood that this cross-section is drawn conventionally showing a portion of several cells of a typical transistor which may include thousands of such cells." However, there is no indication of how these cells are arranged. The cross-sectional views shown in Figures 1-3 of Hshieh could well be part of a structure that is commonly referred to as a "closed cell" array where the trench cells have a polygonal structure, as opposed to a striped structure with the trenches arranged "substantially parallel to each other."

Thus, Hsheih does not disclose a plurality of trenches extending in parallel as set forth in claims 67-96. Claims 67-96, therefore, are further distinguished from Hshieh for this additional reason.

5. <u>Claims 97-120: Hshieh fails to disclose a heavy body having "a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate"</u>

Independent claim 97 and all claims dependent therefrom recite a specific dopant profile for the heavy body as follows: "a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate." This aspect of the present invention is described, for example, at page 9, lines 23-28, and depicted in Figure 5 of the application as originally filed.

The Examiner does not address this element of claims 97-120 in the rejection. There is no mention of any specific doping profile for any P+ body region in any of the embodiments described in Hshieh. To the extent that the rejection applies the inherency argument to claim 97 as well, Appellants traverse that rejection in the same manner as for claims 46 and 67. That is, for the same reasons that Hshieh fails to inherently disclose an abrupt junction, it fails to inherently disclose a "doped heavy body region having a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate."

Appellants respectfully submit that claims 97-120 are therefore further distinguished from Hshieh for this additional reason.

6. Claims 47, 69 and 98: Hshieh fails to disclose that the claimed "location of the abrupt junction...is adjusted"

In rejecting claims 47, 69 and 98, the Examiner states that Hshieh inherently teaches that the "location of the abrupt junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor." The Examiner supports this position in the Office Action dated May 3, 2005 by stating:

> For instance, the depth of the abrupt junction significantly changes in order to control the current that passes through the channel of the device. It should be noted that the electric field which inherently occurs here in is controlled relatively by the magnitude of the current.... Therefore, to control the electric [field] it is inherently to control the current. The current is controlled by the concentration and the thickness of the channel of the transistor. [Office Action, pages 5-6].

Appellants respectfully submit that this reasoning is flawed and is based on a misunderstanding of the nature of the claimed device and its operation. The above claims are directed at adjusting the location of the heavy body junction during fabrication, after which the junction remains at the depth for which it was designed. The depth of the heavy body junction does not vary during the operation of the device. The Examiner however is apparently referring to changes that occur during device operation.

To be clear, claims 47, 69 and 98 recite that the "location of the abrupt junction" is adjusted for the recited purpose and one of skill in the art would readily understand that this is accomplished during fabrication. Contrary to the Examiner's assertion, applying a voltage during device operation does not inherently change the junction's location. The location of the junction is always the same, at the common interface between two regions.

Based on the Examiner's statements above, Appellants speculate that the Examiner is referring to the *width of the depletion region*. The size of the depletion region at the junction between the P-type well and N-type drift region (epitaxial layer) does vary during the operation of the device. However, while the *width of the depletion region* changes with an applied voltage during operation, the "location of the abrupt junction," as recited in claims 47, 69 and 98, does not.

Thus, the rejection fails to provide any objective evidence or cogent technical reasoning to show that the missing descriptive matter—i.e., adjusting the location of the heavy body or the abrupt junction relative to the well junction—is necessarily present in any of the devices disclosed by Hshieh. Accordingly, claims 47, 68 and 98 are further distinguished from Hshieh for this additional reason.

7. Claims 58 and 109: Hshieh fails to disclose the claimed termination structure

Claims 58 and 109 recite a termination structure that "comprises a plurality of concentric trenches surrounding the transistor." In rejecting claims 58 and 109, the Examiner points to Hshieh at column 3, lines 46-48, as disclosing the claimed termination structure. While Hshieh does teach that "each transistor active portion is surrounded by a termination portion, typically including doped regions and sometimes trenches," this teaching is essentially the full extent of Hshieh's disclosure on termination structures. Hshieh, therefore, fails to teach or suggest a termination structure that comprises "a plurality of concentric trenches surrounding the transistor." Claims 58 and 109 are thus further distinguished from Hshieh for this additional reason.

B. The combination of Hshieh and Williams fails to render claims 53, 59, 74-73, 85, 88, 90-91, 96, 104, 110, and 119-120 unpatentable under 35 U.S.C. § 103(a)

Claims 53, 59, and 74-83, 85, 88, 90-91, and 96 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh in view of Williams. In rejecting the claims, the Examiner essentially asserts that all claimed features not disclosed by Hshieh are taught by Williams. In order to establish a *prima facie* case for obviousness, three basic criteria must be met. First, the prior art references must teach or suggest all of the claimed limitations. Second, there must be some suggestion or motivation to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success. *See, e.g.*, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and MPEP 2143. Appellants respectfully submit that the *prima facie* case for obviousness is not met.

Appellants respectfully submit that the combination of Hshieh and Williams fails to get past the first criteria because the combination fails to teach or suggest all of the claimed limitations. The arguments presented above under section VII.A identify a number of claimed features not disclosed by Hshieh. Williams does not cure many of the deficiencies of Hshieh as further explained below.

1. Claims 46-96: The combination of Hshieh and Williams fails to teach or suggest an "abrupt junction"

As discussed above under VII.A.1, Hshieh does not teach or suggest a heavy body region that forms an abrupt junction with the well. Williams similarly fails to teach or suggest an abrupt junction. There is no mention of any junction being abrupt by Williams, and for the same reasons that Hshieh fails to inherently disclose an abrupt junction, Williams fails to inherently disclose an abrupt junction. Williams does include a P+ doped region 317 in Fig. 3; however, as described by Williams, this P+ doped region differs from "conventional body contact regions" in that it does not reach the surface in the plane of Fig. 3. [Williams, col. 5, lines 29-32]. In other words, the P+ doped region 317 is otherwise a "body contact" region - i.e., it is provided for the purpose of making contact to the well (or body) region 320. The variation in the design of this P+ doped region 317 (in that it does not reach the top surface) is for purposes of reducing the size of the mesa (Ysb) which increases cell density. [Williams, col. 5, lines 46-50].

Nothing in Williams suggests that by manipulating features of this P+ doped region 317 (*e.g.*, forming an abrupt junction) one can impact the breakdown voltage of the device. Instead, to the extent Williams does attempt to address the breakdown voltage concern, it teaches providing "a protective diode cell 32" in the form of deep P+ diffusions that operate "to reduce the strength of the electric field across the gate oxide layers 306A, 306B and at the corners of the trenches and limits the formation of hot carriers in the vicinity of the trench." [Williams, col. 4, line 66 to col. 5, line 2]. This protective diode cell 32 "is provided for a selected number of MOSFET cells in a repetitive pattern across the MOSFET." [Williams, col. 5, lines 8-10]. Just as in Hshieh, this indicates that Williams also fails to appreciate the impact of an abrupt junction between a shallow heavy body junction and the well, and therefore does not contemplate such an abrupt junction even though it attempts to address a similar problem.

Thus, neither Hshieh nor Williams, nor the combination thereof, teaches or suggests, inherently or otherwise, a heavy body region that forms an abrupt junction with the well. Claims 46-96 are therefore patentably distinguished from the cited references for at least this reason.

2. <u>Claims 97-120: The combination of Hshieh and Williams fails to teach or suggest the claimed dopant profile for the heavy body</u>

Claims 97-120 recite a heavy body having "a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate." As discussed above under VII.A.5, Hshieh does not disclose the claimed dopant profile in any of its junctions. Williams does not cure this deficiency. The Examiner has not pointed to any disclosure in Williams (or Hshieh) that is relevant to this element of the claims. Nor can the Appellants find any reference to a specific dopant profile for a heavy body region in either Hshieh or Williams. The combination of Hshieh and Williams therefore fails to teach or suggest such dopant profile. Claims 97-120 are thus patentably distinguished over the cited references.

3. Claims 65, 95 and 116: The combination of Hshieh and Williams fails to teach or suggest the claimed "distance between a bottom of the doped heavy body to the doped well junction"

As discussed above under VII.A.3, Hshieh fails to disclose a device wherein "a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5 μm to 1.5 μm" as set forth in claims 65, 95 and 116. Williams does not cure this deficiency. Nowhere in Williams could the Appellants find any disclosure that would teach or even suggest the specific dimensions set forth in these claims. To the extent that the Examiner has argued, in connection with related claims 66 and 117, that dimensional limitations are *prima facie* obvious, Appellants submit that the dimensions recited in claims 65, 95 and 116 are for a particular unobvious purpose. As provided in the detailed description of the present application (*e.g.*, page 6, lines 17-23), the inventors recognized that the depth of the heavy body junction relative to the well junction has an appreciable impact on electric fields in the active area. An advantage gained by designing a device with the relative dimensions as described in the application and set forth in the claims is the improvement in breakdown voltage.

Claims 65, 95 and 116 are therefore further patentably distinguished from the combination of Hshieh and Williams.

4. Claims 47, 69 and 98: The combination of Hshieh and Williams fails to disclose that the claimed "location of the abrupt junction...is adjusted"

Under section VII.A.6 above, Appellants discussed how Hshieh fails to teach, inherently or otherwise, that the "location of the abrupt junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor." Williams does not add anything in this regard. Again, to the extent Williams attempts to address the problem of destructive breakdown, it teaches providing "protective diode cells" repeated across the array of active cells. Nothing in Williams even suggests that the "location" of the junction between P+ region 317 and the underlying well 310 can influence the breakdown voltage of the device.

Thus, the combination of Hshieh and Williams fails to disclose or suggest the claimed location of the heavy body junction relative to the well junction. Accordingly, claims 47, 68 and 98 are further patentably distinguished from the combination of the cited art.

5. Claims 58, 59, 79, 109, and 110: The combination of Hshieh and Williams fails to teach or suggest the claimed termination structure

Under section VII.A.7 above, Appellants discussed how Hshieh fails to teach a termination structure comprising "a plurality of concentric trenches surrounding the transistor" which is recited in claims 58, 79 and 109. Williams does not cure this deficiency. No teaching or suggestion could be found any where in Williams regarding a termination structure having a plurality of concentric trenches. The combination of Hshieh and Williams therefore fails to disclose or suggest a termination structure with a plurality of concentric trenches as recited in claims 58, 79 and 109.

Claims 59 and 110 define a termination structure with a termination trench "wherein the termination trench extends to substantially the same depth as the transistor trench." In rejecting these claims, the Examiner asserts that Williams teaches in Fig. 3 "a deep well 316 that functions as termination region surrounding the device that has a depth extends [sic] to substantially the same depth as the transistor trench," and that it would have been obvious to combine this teaching with the termination structure of Hshieh. Appellants submit that this rejection is based on a misunderstanding of the nature of the device disclosed in Williams. Deep well 316 is simply not a termination structure.

Referring to Williams' description of Fig.3, Williams explains that deep P+ diffusion 316 is "a protective diode" that is "provided for a selected number of MOSFET cells in a repetitive pattern across the MOSFET." [Williams, col. 4, line 57 to col. 5, line 14]. Therefore, deep P+ diffusion is clearly not a termination structure since it does not surround and terminate the active area of the transistor. Neither Williams nor Hshieh, nor their combination teaches or suggests any specific depths for a trench termination structure. Claims 59 and 110 are therefore further patentably distinguished over the cited references.

CONCLUSION

In view of the foregoing remarks, Appellants respectfully request reversal of the rejections of all pending claims.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

46. (previously presented) A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into the semiconductor substrate;

a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction at a first depth;

a doped source region having dopants of the first conductivity type and extending into the semiconductor substrate to form a source junction at a second depth; and

a doped heavy body region having dopants of the second conductivity type and extending into the doped well to form a heavy body junction at a depth that is deeper than the source junction and shallower than the trench,

wherein the heavy body region forms an abrupt junction in the doped well.

47. (previously presented) The field effect transistor of claim 46 wherein a location of the abrupt junction relative to the well junction is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor.

48. (previously presented) The field effect transistor of claim 46 wherein the doped well has a substantially flat bottom.

49. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded top corners.

50. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded bottom corners.

51. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded top and bottom corners.

52. (previously presented) The field effect transistor of claim 46 wherein the heavy body comprises a heavily doped region formed by implanting dopants of the second conductivity type at an approximate location of the abrupt junction.

53. (previously presented) The field effect transistor of claim 46 wherein the trench is lined with a dielectric material and substantially filled with conductive material, wherein the conductive material substantially filling the trench is recessed relative to the surface of the substrate.

54. (previously presented) The field effect transistor of claim 46 wherein the substrate comprises a first highly doped region and a second doped region disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region.

55. (previously presented) The field effect transistor of claim 54 further comprising a termination structure surrounding the transistor.

56. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a doped region having dopants of the second conductivity type extending into the second doped region of the substrate to form a PN junction between the termination doped region and the second doped region of the substrate.

57. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a trench.

58. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a plurality of concentric trenches surrounding the transistor.

59. (previously presented) The field effect transistor of claim 57 wherein the termination trench extends to substantially the same depth as the transistor trench.

60. (previously presented) The field effect transistor of claim 54 wherein the second doped region of the substrate has an initial thickness of less than 10μm.

61. (previously presented) The field effect transistor of claim 54 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is less than 3μm.

62. (previously presented) The field effect transistor of claim 54 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately 1μm.

63. (previously presented) The field effect transistor of claim 46 wherein the depth of the doped well ranges from approximately 1μm to 3μm.

64. (previously presented) The field effect transistor of claim 46 wherein the depth of the doped heavy body ranges from approximately 0.4μm to 1.5μm.

65. (previously presented) The field effect transistor of claim 46 wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5μm to 1.5μm.

66. (previously presented) The field effect transistor of claim 46 wherein a distance between a bottom of the doped heavy body to the doped well junction is less than approximately 0.5μm.

67. (previously presented) A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate, the space between adjacent trenches defining a contact area;

a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction with the substrate;

a doped source region having dopants of the first conductivity type forming a source junction inside the doped well;

a heavy body having dopants of the second conductivity type and extending into the doped well to a second depth that is deeper than the source junction; and

heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction within the doped well.

68. (previously presented) The field effect transistor of claim 67, wherein said doped well has a substantially flat bottom.

69. (previously presented) The field effect transistor of claim 67 wherein a location of the abrupt junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the plurality of gate-forming trenches.

70. (previously presented) The field effect transistor of claim 67 wherein said doped well has a depth less than the first depth of the gate-forming trenches.

71. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded top corners.

72. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded bottom corners.

73. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded top and bottom corners.

74. (previously presented) The field effect transistor of claim 67 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a depth greater than the first depth of the plurality of gate-forming trenches.

75. (previously presented) The field effect transistor of claim 74 wherein the deep doped region forms a PN junction diode with the substrate.

76. (previously presented) The field effect transistor of claim 74 wherein the deep doped region forms a field termination structure surrounding the periphery of the plurality of gate-forming trenches.

77. (previously presented) The field effect transistor of claim 76 further comprising:

a layer of dielectric material formed over the deep doped region; and

a layer of conductive material formed on top of the layer of dielectric material.

78. (previously presented) The field effect transistor of claim 67 further comprising a field termination structure comprising a trench substantially surrounding the plurality of gate-forming trenches.

79. (previously presented) The field effect transistor of claim 78 wherein said field termination structure comprises a plurality of concentrically arranged trenches.

80. (previously presented) The field effect transistor of claim 67 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.

81. (previously presented) The field effect transistor of claim 67 wherein said doped source region extends along the length of the trench.

82. (previously presented) The field effect transistor of claim 81 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contact the doped source region.

83. (previously presented) The field effect transistor of claim 81 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.

84. (previously presented) The field effect transistor of claim 67 wherein between a pair of adjacent trenches a plurality of doped source regions are positioned on opposite sides of each trench, and wherein the heavy body is bounded by the pair of adjacent trenches and the doped source regions.

85. (previously presented) The field effect transistor of claim 67 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.

86. (previously presented) The field effect transistor of claim 67 further comprising:

a layer of dielectric material lining inside walls of each of said plurality of gate-forming trenches; and

a layer of conductive material substantially filling the gate-forming trenches.

87. (previously presented) The field effect transistor of claim 86 wherein the layer of conductive material comprises polysilicon.

88. (previously presented) The field effect transistor of claim 86 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.

89. (previously presented) The field effect transistor of claim 67 wherein the substrate comprises a first highly doped region and a second doped region disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region.

90. (previously presented) The field effect transistor of claim 89 wherein the second doped region of the substrate has an initial thickness of less than 10μm.

91. (previously presented) The field effect transistor of claim 89 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is less than 3μm.

92. (previously presented) The field effect transistor of claim 89 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately 1μm.

93. (previously presented) The field effect transistor of claim 67 wherein the depth of the doped well ranges from approximately 1μm to 3μm.

94. (previously presented) The field effect transistor of claim 67 wherein the depth of the doped heavy body ranges from approximately 0.4μm to 1.5μm.

95. (previously presented) The field effect transistor of claim 67 wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5μm to 1.5μm.

96. (previously presented) The field effect transistor of claim 67 wherein a distance between a bottom of the doped heavy body to the doped well junction is less than approximately 0.5μm.

97. (previously presented) A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into the semiconductor substrate;

a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction at a first depth;

a doped source region having dopants of the first conductivity type and extending into the semiconductor substrate to form a source junction at a second depth; and

a doped heavy body region having dopants of the second conductivity type and extending into the doped well to form a heavy body junction at a depth that is deeper than the source junction and shallower than the trench, the doped heavy body region having a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate.

98. (previously presented) The field effect transistor of claim 97 wherein a location of the heavy body junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor.

99. (previously presented) The field effect transistor of claim 97 wherein the doped well has a substantially flat bottom.

100. (previously presented) The field effect transistor of claim 97 wherein the trench has rounded top corners.

101. (previously presented) The field effect transistor of claim 97 wherein the trench has rounded bottom corners.

102. (previously presented) The field effect transistor of claim 97 wherein the trench has rounded top and bottom corners.

103. (previously presented) The field effect transistor of claim 97 wherein the region of high dopant concentration in said doped heavy body region is formed by implanting dopants of the second conductivity type at an approximate location of the junction with the doped well.

104. (previously presented) The field effect transistor of claim 97 wherein the trench is lined with a dielectric material and substantially filled with conductive material, wherein the conductive material substantially filling the trench is recessed relative to the surface of the substrate.

105. (previously presented) The field effect transistor of claim 97 wherein the substrate comprises a first highly doped region and a second doped region disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region.

106. (previously presented) The field effect transistor of claim 105 further comprising a termination structure surrounding the transistor.

107. (previously presented) The field effect transistor of claim 106 wherein the termination structure comprises a doped region having dopants of the second conductivity type extending into the second doped region of the substrate to form a PN junction between the termination doped region and the second doped region of the substrate.

108. (previously presented) The field effect transistor of claim 106 wherein the termination structure comprises a trench.

109. (previously presented) The field effect transistor of claim 106 wherein the termination structure comprises a plurality of concentric trenches surrounding the transistor.

110. (previously presented) The field effect transistor of claim 108 wherein the termination trench extends to substantially the same depth as the transistor trench.

111. (previously presented) The field effect transistor of claim 105 wherein the second doped region of the substrate has an initial thickness of less than 10μm.

112. (previously presented) The field effect transistor of claim 105 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is less than 3μm.

113. (previously presented) The field effect transistor of claim 105 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately 1μm.

114. (previously presented) The field effect transistor of claim 97 wherein the depth of the doped well ranges from approximately 1μm to 3μm.

115. (previously presented) The field effect transistor of claim 97 wherein the depth of the doped heavy body ranges from approximately 0.4μm to 1.5μm.

116. (previously presented) The field effect transistor of claim 97 wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5μm to 1.5μm.

117. (previously presented) The field effect transistor of claim 97 wherein a distance between a bottom of the doped heavy body to the doped well junction is less than approximately 0.5μm.

118. (previously presented) The field effect transistor of claim 97 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a depth below the trench.

119. (previously presented) The field effect transistor of claim 118 wherein said deep doped region forms a PN junction diode with the substrate.

120. (previously presented) The field effect transistor of claim 119 wherein the deep doped region forms a termination structure.

IX. EVIDENCE APPENDIX - NON-APPLICABLE

X. RELATED PROCEEDINGS APPENDIX - NON- APPLICABLE

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